REMARKS/ARGUMENTS

This Amendment after Final is responsive to the Final Rejection mailed January 10, 2006, rejecting claims 1-9 and 11-15. Claims 1, 14 and 15 have been amended and therefore claims 1-9 and 11-15 remain in this application.

The Examiner's consideration of the prior art including foreign documents 10-512069 and 10-512070 not in the English language, but to the extent he can understand and appreciate the information contained therein, is very much appreciated. Applicant is not in possession of a translation of these documents and neither the Manual of Patent Examining Procedure nor the Code of Federal Regulations require Applicant to obtain a translation.

The Examiner's objection to claim 1 requesting that a dash be inserted between "multiple" and "data" has been obviated by the cancellation of this phrase. However, the Examiner's proposed correction to claim 15 has been included in the above amendment (correcting the spelling of "operation").

Claims 1-9 and 11-15 stand rejected under 35 USC §103 as unpatentable over JP 5-88887 (cited by Applicant in an Information Disclosure Statement) and Chan (U.S. Patent 5,276,881). Applicant has modified independent claims 1, 14 and 15 by specifying that the second portion of bit length B of the data word Rm is subjected to an arithmetic right shift where the right shift has a shift amount specified by said shift operand and is independent of said bit length A of said first portion of the data word. Support for this limitation is set out in Applicant's specification, page 5, lines 6-7, which states that "the PKHTB instruction of Figure 3 takes a fixed top half of one input operand data word stored in the register Rn and a variable positive half bit-portion of a second input operand data word stored in the register Rm . . . ." (See Applicant's specification,

page 7, lines 6-8). This is also disclosed with respect to the embodiment of Figure 4 on page 7, lines 10 and 11 specifying that "the instruction PKHBT takes the bottom half of an input operand data word of Rn and a variable position half word length portion of a second input operand data word of Rm . . . ."

Thus, the amendment to claims 1, 14 and 15 emphasizes that the present invention addresses the problem of increasing efficiency by which a data processing system performs data processing operations by combining additional data manipulation with a packing operation such that one of the portions to be combined into a packed output data word can be multiplied or divided by a power of 2 at the same time it is being packed together with another data word portion. This invention enables flexibility in defining the additional data manipulation by allowing one of the data words being packed to be selected from a variable position within its input operand data word such that the shift amount specified by the shift operand (to which the second portion of a data word Rm is subjected) is independent of the bit length A of the first portion of the other data word Rn with which it is combined to form the output data word.

JP 5-88887 discloses on page 7, lines 13-15, that "low-order key bits of the general register Rn and all bits fo the general register Rm or the memory 30 are linked and rotated k bits left" when the Rotate Multi bit Left (RML) instruction is executed. Looking at Figure 4 on page 738 of JP 5-88887, it can be seen that at stage (3) data in the shift register SR1 is right-shifted by ten bits and the contents in shift registers SR1 and SR2 are then linked to each other and shifted ten bits left (as discussed in JP 5-88887, page 8, lines 6-9). Thus, JP 5-88887 teaches away from Applicants' independent claims 1, 14 and 15 because in JP 5-88887, the shift size k is equal to the number of bits selected from the general register Rn. The number of bits preserved

in the shift register SR1 is always 16 bits and therefore cannot disclose or render obvious the subject matter of Applicant's independent claims where the arithmetic right-shift is an amount specified by the shift operand independent of bit length A of the first portion.

The advantages of Applicant's claimed variable shifting is that it is independent of the bit length of the portion of the other (unshifted) data word, as discussed in Applicant's specification on page 7, lines 22-25. The claimed invention therefore provides a data processing apparatus that is capable of performing changes in the "Q" values in a manner that is much more flexible and powerful than the circuit taught in JP 5-88887.

Moreover, the Examiner has simply failed to meet his burden of demonstrating any "reason" or "motivation" for combining the JP 5-88887 reference with the Chan reference. In order to establish a *prima facie* basis for an obviousness rejection, it is incumbent upon the Examiner to establish how or why there is some reason or motivation for combining these two references. In the present instance, the Examiner merely draws the conclusion that it would be obvious without providing any reason or motivation for picking and choosing elements of the JP and Chan references and then combining them in the manner of Applicant's claims. Accordingly, any further rejection of claims 1-9 and 11-15 as amended above is respectfully traversed.

Entry of the Amendment pursuant to the provisions of 37 CFR 1.116

Applicant has made the minor corrections in claims 1 and 15 as suggested by the Examiner. Additionally, Applicant has amended all three independent claims to more positively recite the flexible shifting amount feature which provides the increased data processing efficiency of Applicant's invention. This aspect is also emphasized as it is the feature which the

JP 5-88887 reference leads those of ordinary skill in the art away from. Inasmuch as JP 5-88887 was cited in Applicant's previously submitted Information Disclosure Statement, Applicant was well aware of this reference when drafting the above claims.

No new issue can be raised by the entry of the above limitation

Applicant understands that the language of section (iii) of independent claim 1 (and similar portions of claims 14 and 15) read in means-plus-function format, i.e., "an instruction decoder . . . for performing an operation . . . ." No structure is recited in the claim which performs the recited function and thus, under the Federal Circuit guidelines, such claims are to be construed as "means plus function" claims, even in the absence of use of the word "means."

As such, the Examiner is bound to construe this claim in accordance with the sixth paragraph of 35 USC §112 as covering the corresponding structure set out in Applicant's specification and equivalents thereto. The corresponding structure in Applicant's specification provides an "arithmetic right-shift having a shift amount specified by said shift operand being independent of said bit length A of said first portion." Thus, the proper construction of the claimed "instruction decoder . . . for performing an operation . . . " is to include this limitation set out in Applicant's specification.

However, it would appear that the Examiner has not construed the claim to include this limitation and therefore has improperly construed the claim language. Rather than seeking review of the Examiner's improper claim construction from the Board, Applicant offers the above amendment positively reciting this variable shift limitation to independent claims 1, 14 and 15, which limitation should obviate the need for any appeal and yet should meet the Examiner's requirement for positively defining over the cited prior art of record. However, the

fact that applicant offers this amendment does not and should not be taken as an admission that applicant believes this limitation is not already contained in the existing language of the claim, when properly construed.

Given the possibility that the Examiner may not construe this claim language as "means-plus-function" language, the Examiner's attention is directed to the Court of Appeals for the Federal Circuit cases in which the absence of the word "means" does not avoid means-plus-function statutory language. Instead, it is whether the claim recites structure which will perform the recited functions. It is noted that claim 1, while it recites an instruction decoder, does not recite the structure for "performing an operation upon a data word Rn and a data word Rm, ..." Thus, even though the word "means" is not used, the language of section (iii) in independent claim 1 is in means-plus-function format and therefore must be construed in accordance with Applicant's specification and equivalents of that corresponding disclosed structure.

Entry of the above amendment clarifying the proper construction of Applicant's independent claims does not raise any new issue, as this issue should already have been considered by the Examiner when properly construing the means-plus-function language of claims 1, 14 and 15. However, Applicant offers the above amendment in order to direct the Examiner's attention to this claim construction problem in the present case and as away of clearly evidencing the scope of Applicant's independent claims.

Entry of the above amendment also should not only overcome claim objections set out in the outstanding Official Action, but place the independent claims and all claims dependent thereon in condition for allowance, thereby obviating the need for any further appeal.

SYMES
Appl. No. 09/960,728
April 10, 2006

In order to provide sufficient time for the Examiner's consideration of this Rule 116 Amendment, Applicant has re-noted the Appeal in this case, but has forwarded this Amendment under Rule 116 by fax and requests the Examiner's early consideration thereof. Obviously, the Examiner's contacting Applicant's undersigned representative and indicating the disposition of this Rule 116 Amendment in a timely manner would be appreciated, i.e., well before the June 10, 2006 date for filing an Appeal Brief.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that claims 1-9 and 11-15 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of these claims, he is respectfully requested to contact Applicant's undersigned representative.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____
Stanley C. Spooner
Reg. No. 27,393

SCS:kmm
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100